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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,702	01/21/2004	Meng-Hung Chen	10113671	3361

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QUINTERO LAW OFFICE
1617 BROADWAY, 3RD FLOOR
SANTA MONICA, CA 90404

EXAMINER	
WARREN, MATTHEW E	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,702	CHEN, MENG-HUNG	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on July 11, 2005.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on March 14, 2005 is being considered by the examiner. However, the US reference (US 6,006,569) listed in that IDS does not have the same publication date (05-23-2000) as listed. US Patent 6,006,569 is a patent issued to Shrayer et al. on 12-28-1999 and pertains to a "Method For Manufacturing A Dome From An Undersized Blank." It seems that the reference has been cited incorrectly, is not relevant to the instant invention, and therefore was not considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-9, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figure 3E (APAF) in view of Maex et al. (US 6,323,555 B1).

In re claim 1, the APAF 3E shows a bit line contact structure, comprising: a substrate 100 having a transistor thereon, the transistor having a gate electrode 120,

drain region 132, and source region 134; a dielectric layer 140, the dielectric layer having an opening 142 exposing the drain region; and a conductive layer in the opening. The dielectric layer is formed directly on the transistor. The APAF shows all of the elements of the claims except the dielectric being a composite layer. Maex et al. shows (fig. 1H) a contact structure having a composite dielectric layer comprising a first dielectric layer 2, a barrier layer 3, and a second dielectric layer formed on the substrate. The first dielectric comprises a spin coating material (col. 1, line 62-col. 2, line 8). The first dielectric may also be a polyimide (col. 5, lines 1-21). The composite dielectric has an opening exposing the surface of the substrate and a conductive layer 8 is formed therein. This configuration of composite interlayer dielectrics allows for a semiconductor device having a low-K dielectric with improved gap filling and planarization. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the dielectric layer of the APAF by forming a composite layer as taught by Maex to provide a semiconductor device having a low-K dielectric with improved gap filling and planarization.

In re claims 4 and 6, Maex discloses (col. 6, lines 33-67)that the first dielectric is fluorinated polyimide, the barrier is SiN and the second dielectric comprises oxide (the second dielectric is made of the same materials as the first layer, which includes oxide).

In re claim 8, Maex discloses (col. 7, lines 20-25) that the conductive layer is copper.

In re claims 3, 5, 7, and 9, none of the references disclose the specific dimensions of the dielectric layers or the conductive layer. However, it would have been

obvious to one of ordinary skill in the art to make the thickness of the dielectric layers and the conductive layer within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

In re claim 27, Maex discloses (col. 5, lines 1-21) that the first dielectric comprises fluorinated polyimide.

Claims 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figure 3E (APAF) in view of Maex et al. (US 6,323,555 B1) and Hedrick et al. (US Pub. 2004/0207084 A1).

In re claim 25, the APAF 3E shows a bit line contact structure, comprising: a substrate 100 having a transistor thereon, the transistor having a gate electrode 120, drain region 132, and source region 134; a dielectric layer 140, the dielectric layer having an opening 142 exposing the drain region; and a conductive layer in the opening. The dielectric layer is formed directly on the transistor. The APAF shows all of the elements of the claims except the dielectric being a composite layer. Maex et al. shows (fig. 1H) a contact structure having a composite dielectric layer comprising a first dielectric layer 2, a barrier layer 3, and a second dielectric layer formed on the substrate. The first dielectric comprises a spin coating material (col. 1, line 62-col. 2, line 8). The first dielectric may also be a polyimide (col. 5, lines 1-21). The composite dielectric has an opening exposing the surface of the substrate and a conductive layer 8 is formed therein. This configuration of composite interlayer dielectrics allows for a

semiconductor device having a low-K dielectric with improved gap filling and planarization. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the dielectric layer of the APAF by forming a composite layer as taught by Maex to provide a semiconductor device having a low-K dielectric with improved gap filling and planarization.

Neither reference discloses that the first layer is polysilsesquioxane, however, polysilsesquioxane is one of many known materials in the art. However, Hedrick et al. discloses [0030] that polysilsesquioxane is one of many known spin-on materials having a low dielectric constant. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the spin-on polyimide first dielectric layer of the APAF and Maex with polysilsesquioxane as taught by Hedrick to form a suitable dielectric layer having a low dielectric constant.

Response to Arguments

Applicant's arguments filed with respect to claims 1-9 have been fully considered but they are not persuasive. The applicant primarily asserts that Maex cannot be combined with the APAF because the motivation for combining differs from the motivation of the applicant's claimed invention. In response to applicant's argument that Maex does not solve the problem of voids as taught in the APAF, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. &

Inter. 1985). Furthermore, the gap filling taught in Maex does pertain to the problem of the APAF. If voids are a problem in the invention, then a material with good gap filling capability would be useful in also filling voids, since voids and gaps are the same thing. Maex also teaches the same materials as the instant invention, therefore, those materials would inherently have the same properties and functions as the instant invention. Although Maex does not show the transistor having the gate electrode and source and drain regions formed on the substrate, it is well known in the art that interlayer dielectrics are usually formed on or over transistors. For Maex, the complete device is not shown but the invention is still applicable since it pertains to covering of the substrate and adhesion to subsequent contact structures. Therefore, the cited references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

MEW

SUPERVISOR

October 13, 2005